UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/752,243	12/28/2000	Nicholas G. Samra	2207/10613	7462

7590 12/01/2005

KENYON & KENYON
333 W. San Carlos, Street, Suite 600
San Jose, CA 95110-2711

EXAMINER	
MEONSKE, TONIA L	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 12/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/752,243	SAMRA, NICHOLAS G.	
	Examiner	**Art Unit**	
	Tonia L. Meonske	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 14, 16, 17, 19, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Hammerstrom, US Patent 5,369,773.

2. Referring to claim 1, Hammerstrom has taught

a. a physical zero register which reads as a zero value to be used with an instruction set architecture without a dedicated zero register (abstract, Figure 2, Figure 6, column 4, lines 30-68, Element 36 is the claimed physical zero register. There is no dedicated zero register, virtual zeros instead are created.);

b. a Register Alias Table (RAT) for storing an instruction register map (Figure 2, element 34, column 5, lines 12-19); and

c. a Zeroing Instruction Logic (ZIL) unit for detecting a zeroing instruction (column 4, lines 42-68, Figures 2 and 3, The LSB of the lowest virtual register is checked. When the LSB is "0" the read is a zeroing instruction.), deleting the zeroing instruction (column 4, line 42-column 5, line 6, Figures 2 and 3, The data read out and in is ignored.), and modifying the subsequent instruction to account for the deleted zeroing instruction (Figure 2, column 4, lines 42-68, Figures 2 and 3, column 4, line 42-column 5, line 42, A

certain number of subsequent read instructions are modified to read as zero based on the virtual zero counter, element 38.).

3. Referring to claim 14, Hammerstrom has taught

a. a physical zero register which reads as zero to be used with an instruction set architecture without a dedicated zero register (abstract, Figure 2, Figure 6, column 4, lines 30-68, Element 36 is the claimed physical zero register. There is no dedicated zero register, virtual zeros instead are created.);

b. a Zeroing Instruction Logic (ZIL) to read a plurality of instructions and to detect and modifying a zeroing instruction within said plurality of instructions (column 4, lines 42-68, Figures 2 and 3, The LSB of the lowest virtual register is checked. When the LSB is "0" the read is a zeroing read instruction where the instruction and possibly a certain number of subsequent read instructions are modified to read as zero.);

c. where said ZIL unit is to delete said zeroing instruction and set a pointer to said physical zero register in place of said deleted zeroing instruction (column 4, line 63-column 5, line 19, Phantom addresses are provided.); and

d. where said ZIL unit modifies instructions dependent on said deleted zeroing instruction (Figure 2, column 4, lines 42-68, Figures 2 and 3, column 4, line 42-column 5, line 42, A certain number of subsequent read instructions are modified to read as zero based on the virtual zero counter, element 38.).

4. Referring to claim 16, Hammerstrom have taught an apparatus in accordance with claim 14, as described above and wherein said ZIL unit modifies instructions dependent on said deleted zeroing instruction with a renameable pointer (column 5, lines 12-19, phantom addresses).

5. Referring to claim 17, Hammerstrom has taught a method of zero-generating comprising:

a. detecting a zeroing instruction in an instruction set architecture without a dedicated zero register (abstract, Figure 2, Figure 6, column 4, lines 30-68, Element 36 is the claimed physical zero register. There is no dedicated zero register, virtual zeros instead are created.);

d. deleting the zeroing instruction (column 4, line 42-column 5, line 6, Figures 2 and 3, The data read out and in is ignored.);

e. identifying a subsequent instruction using said zeroing instruction (Figure 2, column 4, lines 42-68, Figures 2 and 3, column 4, line 42-column 5, line 42, A certain number of subsequent read instructions are modified to read as zero based on the virtual zero counter, element 38.); and

f. modifying said subsequent instruction with a pointer to a physical zero register which reads as a zero value (Figure 2, column 4, lines 42-68, Figures 2 and 3, column 4, line 42-column 5, line 42, A certain number of subsequent read instructions are modified to read as zero based on the virtual zero counter, element 38.).

6. Referring to claim 19, Hammerstrom has taught a method of claim 17, as described above, and further comprising: modifying said subsequent instruction involves replacing instruction sources (Figure 2, Figures 2 and 3, column 4, line 42-column 5, line 42, A certain number of subsequent read instructions, or sources, are modified to read as zero based on the virtual zero counter, element 38.).

7. Referring to claim 20, Hammerstrom has taught a method of claim 17, as described above, and further comprising: modifying said subsequent instruction involves using a move

(MOV) instruction (Figure 2, Figures 2 and 3, column 4, line 42-column 5, line 42, Zeros are moved to the arithmetic units for execution.).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2 and 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hammerstrom, US Patent 5,369,773.

9. Referring to claim 2, Hammerstrom has taught an apparatus in accordance with claim 1, as described above, and wherein:

a. Hammerstrom has not specifically taught wherein said physical zero register is a read only memory. However, since Hammerstrom is required to create virtual zeros to output for processing, Hammerstrom must guarantee that the value output is always a zero in virtual zero mode. ROM is read only memory, or that the value that it is can never be overwritten. So having a zero value be stored in ROM necessarily guarantees the when that ROM location is read, it will always be zero. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the physical zero register of Hammerstrom, be a ROM, for the desirable purpose of always guaranteeing a zero value output when a virtual zero value is requested.

10. Referring to claims 9-12, Hammerstrom has not specifically taught wherein said zeroing instruction is an exclusive or, a subtraction, a multiply, or a move instruction. However, it's

obvious that the zeroing instruction could be any instruction, such as an exclusive or, a subtraction, a multiply, and a move instruction, which yields the logical equivalent of zero in a destination register. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the zeroing instruction of Hammerstrom be an exclusive or, a subtraction, a multiply, or a move instruction, that yields a value of zero in the destination, as they are all logically equivalent instructions.

11. Claims 3-8, 13, 15, 18, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hammerstrom, US Patent 5,369,773, in view of Rotenberg et al., Trace Cache: A Low Latency Approach to High Bandwidth Instruction Fetching (herein referred to as Rotenberg).

12. Referring to claim 3, Hammerstrom has taught an apparatus in accordance with claim 1, as described above. Hammerstrom has not specifically taught wherein said ZIL unit detects said zeroing instruction in a trace cache line. However, having the apparatus of Hammerstrom implemented in a trace cache processor, such as that taught by Rotenberg, allows the apparatus to employ aggressive techniques to exploit instruction level parallelism (Rotenburg, page 24, section 1 entitled "Introduction", page 25, section 1.1 entitled "The trace cache"). Combining the apparatus of Hammerstrom with the trace cache processor of Rotenberg necessarily yields the ZIL detecting said zeroing instruction in a trace cache line. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the ZIL unit, as taught by Hammerstrom, detect said zeroing instruction in a trace cache line of Rotenburg, for the desirable purpose of employing aggressive techniques to exploit instruction level parallelism (Rotenburg, page 24, section 1 entitled "Introduction", page 25, section 1.1 entitled "The trace cache").

13. Referring to claim 4, Hammerstrom has taught an apparatus in accordance with claim 3, as described above and further comprising: an r0 register field logically coupled to said trace cache line for mapping to said physical zero register (For the above combination of references to work as explained above, the virtual zero register must be coupled to the trace cache line of Rotenburg for mapping to said virtual zero.).

14. Referring to claim 5, Hammerstrom has taught an apparatus in accordance with claim 3, as described above, and wherein said RAT and said trace cache line are logically coupled to a renaming unit for maintaining said pointer to said physical register (For the above combination of references to work as explained above, then the RAT and said trace cache line must be logically coupled to the renaming unit for maintaining the pointer to the physical register.).

15. Referring to claim 6, Hammerstrom has taught an apparatus in accordance with claim 3, as descried above. Hammerstrom have not specifically taught wherein said ZIL unit deletes said zeroing instruction from said trace cache line. However, Hammerstrom have taught deleting the zeroing instruction. Since the zeroing instruction is no longer an instruction that needs executed as Hammerstrom has deleted the instruction, it follows that the ZIL needs to delete the zeroing instruction in the trace line as the zeroing instruction is no longer necessary to be executed. Therefore it would have been obvious to one of ordinary sill in the art at the time the invention was made to delete the zeroing instruction in the trace line as the instruction does not need to be executed and should not be included in the trace of instructions to be executed.

16. Referring to claim 7, Hammerstrom has taught an apparatus in accordance with claim 6, as described above and wherein said ZIL unit modifies a subsequent instruction (Figure 2, column 4, lines 42-68, Figures 2 and 3, column 4, line 42-column 5, line 42, A certain number of

subsequent read instructions are modified to read as zero based on the virtual zero counter, element 38), where said subsequent instruction is logically coupled to said zeroing instruction within said trace cache line (A zeroing instruction and all adjacent subsequent instructions are logically coupled. Having the combination of Hammerstrom and Rotenberg necessarily yields that the claimed subsequent instruction is logically coupled to said zeroing instruction within said trace cache line.).

17. Referring to claim 8, Hammerstrom has taught an apparatus in accordance with claim 7, as described above, and wherein said ZIL unit modifies said subsequent instruction with an immediate source of zero (Figure 2, column 4, lines 42-68, Figures 2 and 3, column 4, line 42-column 5, line 42, A certain number of subsequent read instructions are modified to read as zero based on the virtual zero counter, element 38).

18. Referring to claim 13, Hammerstrom has taught an apparatus in accordance with claim 7, as described above and wherein said ZIL unit transforms said subsequent instruction to a MOV instruction (Figure 2, Figures 2 and 3, column 4, line 42-column 5, line 42, Zeros are moved to the arithmetic units for execution.).

19. Referring to claim 15, Hammerstrom has taught an apparatus in accordance with claim 14, as described above. Hammerstrom has not taught wherein said ZIL unit modifies instructions dependent on said deleted zeroing instructions with an immediate source of a value when both occur with a single trace cache line. However, having the apparatus, as taught by Hammerstrom, implemented in a trace cache processor would allow the apparatus to employ aggressive techniques to exploit instruction level parallelism (Rotenburg, page 24, section 1 entitled "Introduction", page 25, section 1.1 entitled "The trace cache"). Furthermore, one would

want to optimize the instructions and data storage of Hammerstrom in all cases, including when the instructions appear in a singe trace cache line. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the ZIL unit of Hammerstrom modify instructions dependent on said deleted zeroing instructions with an immediate source of a value when both occur with a single trace cache line, in order to employ aggressive techniques to exploit instruction level parallelism and efficient data storage when both instructions appear in a single cache line (Rotenburg, page 24, section 1 entitled "Introduction", page 25, section 1.1 entitled "The trace cache").

20. Referring to claim 18, Hammerstrom has taught a method in accordance with claim 17, as described above. Hammerstrom has not specifically taught pointing to a physical zero register where said subsequent instruction is not within a common trace cache line. However, having the apparatus, as taught by Hammerstrom, implemented in a trace cache processor would allow the apparatus to employ aggressive techniques to exploit instruction level parallelism (Rotenburg, page 24, section 1 entitled "Introduction", page 25, section 1.1 entitled "The trace cache"). Furthermore, one would want to optimize the instructions and data storage of Hamerstrom in all cases, including when said subsequent instruction is not within a common trace cache line. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Hammerstrom point to a physical zero register where said subsequent instruction is not within a common trace cache line in order to employ aggressive techniques to exploit instruction level parallelism and efficient data storage when both instructions are not within a common trace cache line (Rotenburg, page 24, section 1 entitled "Introduction", page 25, section 1.1 entitled "The trace cache").

21. Referring to claim 21, Hammerstrom has taught a method in accordance with claim 17, as described above. Hammerstrom has not specifically taught wherein said subsequent instruction is modified in response to its location in a trace cache relative to said zeroing instruction. However, having the apparatus, as taught by Hammerstrom, implemented in a trace cache processor would allow the apparatus to employ aggressive techniques to exploit instruction level parallelism (Rotenburg, page 24, section 1 entitled "Introduction", page 25, section 1.1 entitled "The trace cache"). Furthermore, since the zeroing instruction is an instruction that no longer needs to be executed, as Hammerstrom has effectively deleted the instruction. It follows that the ZIL needs to delete the zeroing instruction in the trace line as the zeroing instruction is no longer necessary to be executed. Therefore it would have been obvious to one of ordinary sill in the art at the time the invention was made to delete the zeroing instruction in the trace line as the instruction is not executed and should not be included in the trace of instructions to be executed. As a result, the subsequent instruction must be modified in response to its location in a trace cache relative to said zeroing instruction in order to delete the zeroing instruction from the trace cache line and move up the location of a subsequent actual instruction in the trace cache.

Response to Arguments

22. Applicant's arguments with respect to claims 1-21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, with every other Friday off.

24. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dov Popovici can be reached on (571) 272-4083. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

25. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

DOV POPOVICI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100